*Lab. 1*

# Modeling and Simulation of Single Event Transients in CMOS Circuits

**Aim of the lab:** In this exercise, students are introduced to the modeling and characterization of Single Event Transient (SET) effects in CMOS circuits. Using the LTSpice simulator, the SET current model should be implemented in a given circuit in order to simulate the SET effects at the transistor level.

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**Theoretical background:** The performance of CMOS integrated circuits can be degraded due to radiation exposure. One of the most common radiation-induced effects are the Single Event Transients (SETs), which are typically induced in combinational circuits. SETs occur when a single high-energy particle, such a proton, neutron, alpha particle or heavy ion, interacts with a radiation-sensitive component in a target circuit. The most sensitive transistors in a CMOS circuit are the off-state PMOS and NMOS transistors. SET manifests as a current pulse flowing through the affected component. As a result of the induced current pulse, a voltage pulse (SET voltage pulse) may be formed across the target circuit node. The SET voltage pulses may propagate through a combinational logic, and eventually be captured by a sequential element (e.g. flip-flops), which may result in data corruption and malfunction of the circuit or entire system.

The shape of the SET pulse depends on radiation conditions (type and energy of incident particle, strike location and angle of incidence), design parameters (transistor size, load capacitance) and operating parameters (supply voltage, temperature). A particle-induced voltage pulse is considered as an SET pulse if its amplitude exceeds the half of supply voltage (Vdd/2). A minimum particle-induced charge which can cause an SET is known as the critical charge. Alternatively, the deposited energy is expressed in terms of Linear Energy Transfer (LET), i.e., the energy lost by a particle as it passes through the material. The minimum value of

LET required to cause an SET is known as the threshold LET (LETth), and it is linearly proportional to critical charge.

There are various models for the circuit-level (SPICE) simulation of SET effects [1]. In this lab, the model proposed by Kauppila et al. [2], will be used (Fig. 1). This is one of the most advanced compact SET current models, providing a realistic shape of the current pulse as a function of LET. The model is composed of a bias-independent double-exponential current source, two voltage-controlled current sources, and a capacitor that stores particle-induced charge. The model is defined by three parameters which can be varied in simulations: LET, rise time of current pulse (several to tens of ps), and fall time of current pulse (tens for hundreds of ps).

The SET current model is applied in the form of a current source, which is connected between the target circuit node and the supply or ground connection. A typical setup for SET simulations in a target inverter is illustrated in Fig 2.

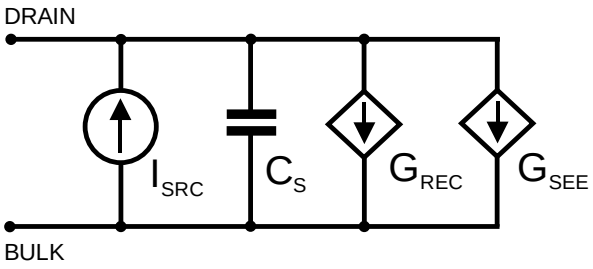


Fig. 1. SET model proposed by Kauppila et al. [2]

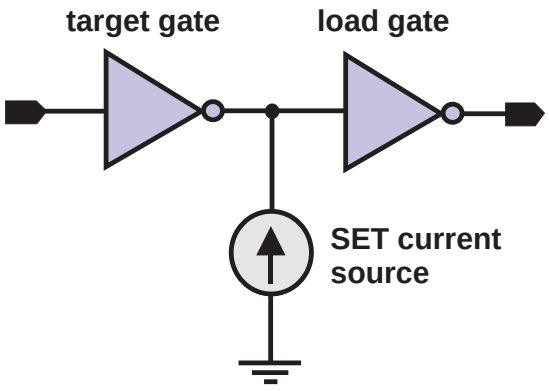


Fig. 2. Insertion of SET current source at the output of inverter

**Realization of the lab:**

1. Download and install the free LTSpice simulation program from the link: https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html
2. After starting the program, open a new schematic (File / New Schematic) and draw a circuit with the NMOS transistor given in Fig. 3. In addition to the highlighted symbols in the palette at the top of the window, the symbols of all components can be reached by clicking on the (Components) icon. For NMOS transistor use symbol NMOS4, and for generators Voltage. Setting the component values is done by right-clicking on the component symbol. Set the values of generator V2 to 1.2V and resistor R1 to 10kΩ.

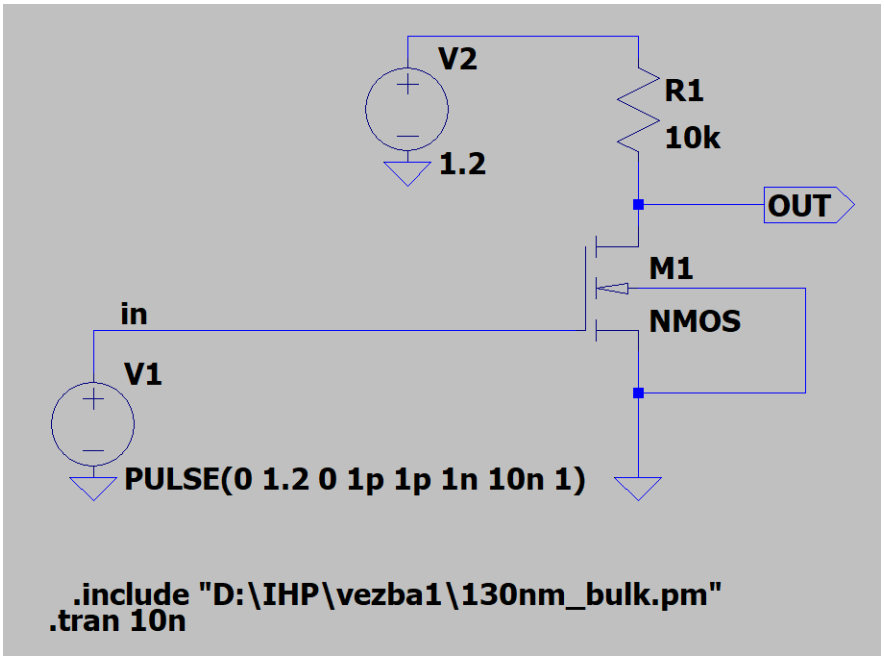


Fig. 3. NMOS circuit schematic

3. Generator V1 will be set to generate a voltage pulse. The setting is made by right-clicking on the generator symbol V1 and the Advanced button. Select PULSE signal and enter signal parameters (Fig. 4). Then click OK.

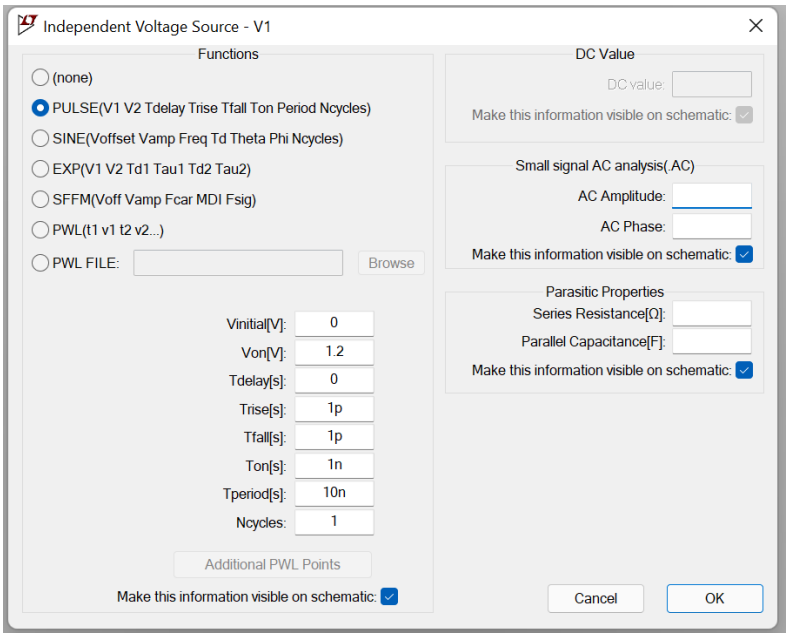


Fig. 4. PULSE voltage source settings

4. Save the project in the desired folder: File / Save As. The file extension should be * .asc.
5. Download the library with the transistor model in 130 nm CMOS technology, from the link: https://ptm.asu.edu/. The model is located in the Latest Models tab, then the downloaded file marked as 130 nm BSIM4 model card for bulk CMOS V1.0. Save the file in the same folder as the previous LTSpice project. Right-click on the file and click on *Copy as Path* to copy the file path.
6. In LTSpice, clicking on the ***.op*** icon opens a window for entering SPICE directives. Enter *.include* and below the path of the file with the transistor model (Fig. 5). The model name is NMOS so it is not necessary to further change the model name on the schematic.

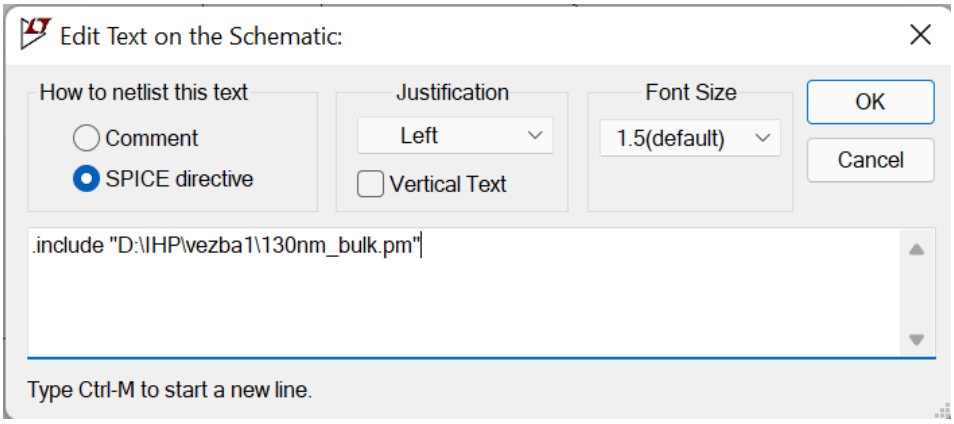


Fig. 5. SPICE directive seetings

7. Adjust the dimensions of the transistor by right-clicking on the symbol. For example, a channel length of 130 nm and a channel width of 1µm (Fig. 6).

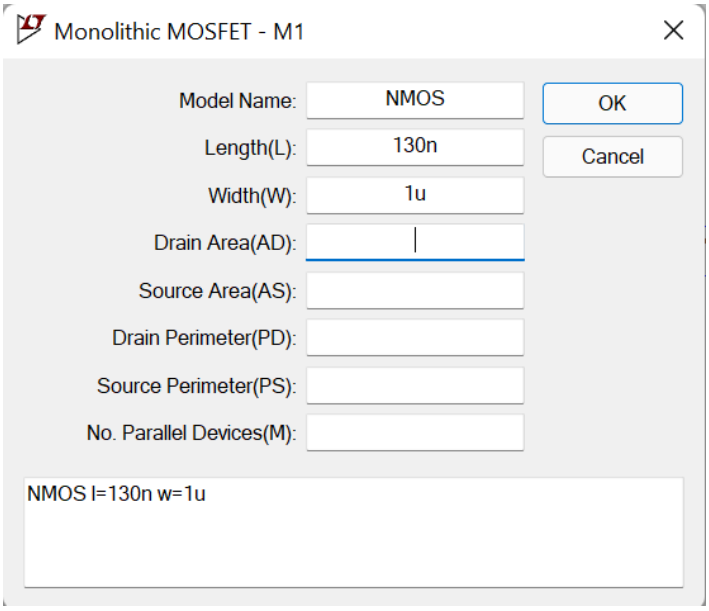


Fig. 6. MOS transistor dimensions settings

8. To start the simulation click on  . Select the desired simulation type and enter the required parameters. In this example, we will do a time analysis of the circuit, so it is enough to enter Stop Time of 10ns within the *Transient* tab (Fig. 7). A window opens to display the simulation results.

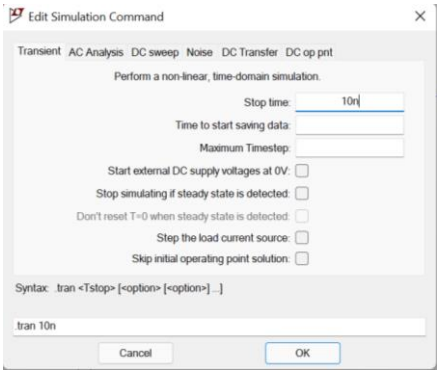


Fig. 7. Edit Simulation Command

9. By placing the cursor on certain nodes in the circuit, the probe symbol appears, clicking on the desired node in the circuit will display the corresponding voltage. To display the current, the cursor should be placed over the component symbol, or at the pin of the transistor. To display the power dissipated on a specific component, simultaneously click ***Alt*** on the keyboard and the desired component symbol.

10. We will analyze the simulation results (Fig. 8). When the input signal ***in*** is high (logic 1), the output voltage of the circuit is low voltage level (logic 0) and vice versa, therefore, this circuit is an NMOS inverter. When there is a logic 1 at the input, the transistor is in ***on*** state, it acts as a closed switch, so that GND voltage appears at the output. When the input is logic 0, the transistor is in the ***off*** state, so the output voltage VDD appears via the pull-up resistor R1.

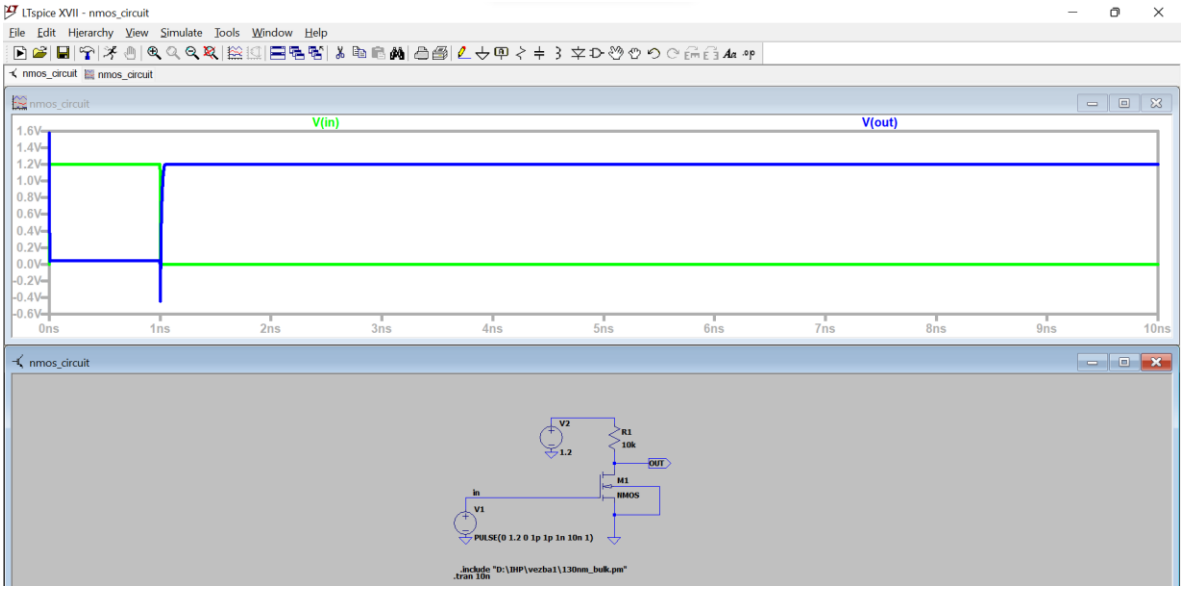


Fig. 8. Simulation results

11. The disadvantage of this circuit is that power consumption occurs when the output signal is logic 0. To confirm this with a simulation, we will add another window to display the results: Plot Settings / Add Plot Pane and display the drain current of the transistor (Fig. 9) or right click on the plot, and select Plot Pane.

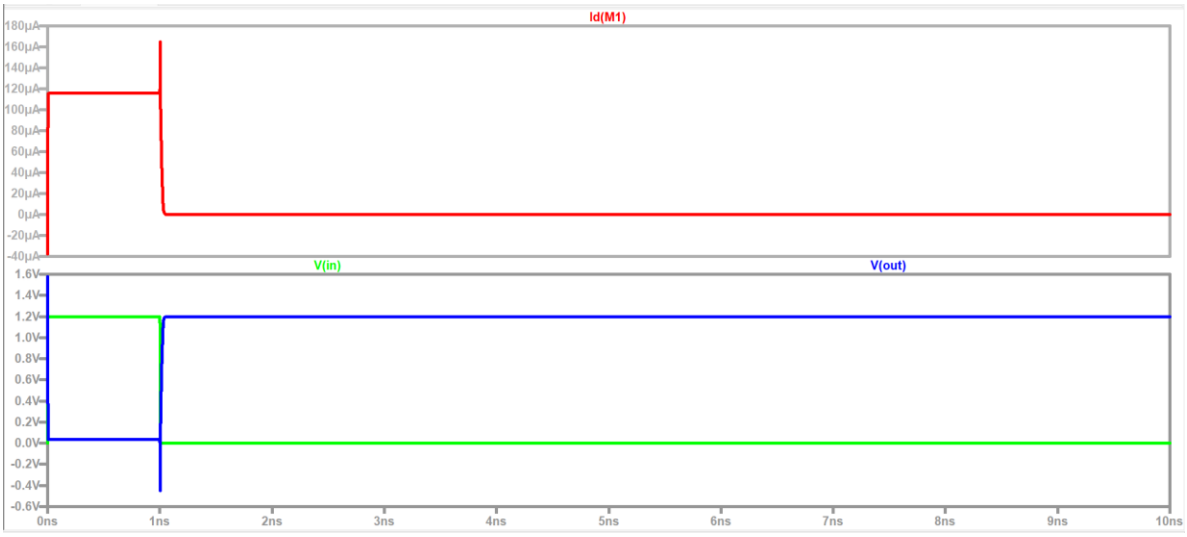


Fig. 9. Simulation results (2)

12. When such a transistor is an integral part of an integrated circuit and is in the ***off*** state, the SET will cause its unwanted switching ***on***. To simulate this we need to create a SET generator. The SPICE netlist of the SET model as a subcircuit is given below and can be downloaded from the following link: https://www.dropbox.com/s/82w2me3kau96px5/CSOUmodel.cir?dl=0.
    In this case, the timing parameters of the current pulse are tau 1 = 10 ps (rise time of current pulse), tau2 = 100 ps (fall time of current pulse).

```
.subckt csou n p tau1=10e-12 tau2=100e-12 TD1=500ps dur=1.5ps let={let1} col_len=1.5e-6 rec=1E11
.params TD2=TD1+dur
.params IMAX=(let*1.035E-2*col_len*1E6*1E-12)/((dur+tau2-tau1)-(tau2-tau1)*exp(-1*(dur/tau1)))
.params F=0.01 CS=1e-12

C1 vc 0 {CS}
I1 0 vc EXP(0 {IMAX} 500p 10e-12 {TD2} 100e-12)
G1 vc 0 value={V(vc)*CS*rec}
G2 vc 0 value={V(vc)*(CS/tau1)*(1.0/(1.0+exp((V(p)-V(n)+3*F)/F)))}
G3 n p value={V(vc)*(CS/tau1)*(1.0/(1.0+exp((V(p)-V(n)+3*F)/F)))}

.ends
```

13. The SET generator symbol needs to be created: File / New Symbol. The symbol is drawn from the elements available in the Draw tab, such as Line, Circle ... After drawing the symbol, pins should be added to it: Edit / Add Pin / Port. Enter *n* and *p*, respectively, in the Label field, since these are the names of the pins in the SET model (Fig. 10).

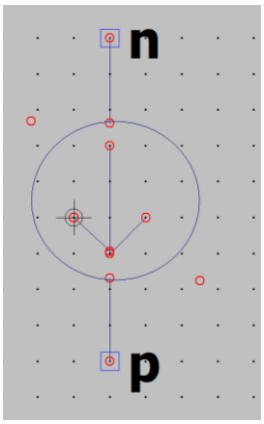


Fig. 10. SET symbol

14. The following is the assignment of the netlist to the symbol: Edit / Attributes / Edit Attributes. The name of the subcircuit should be entered in the field Value, and the path to the subcircuit should be entered in the field ModelFile (Fig. 11).

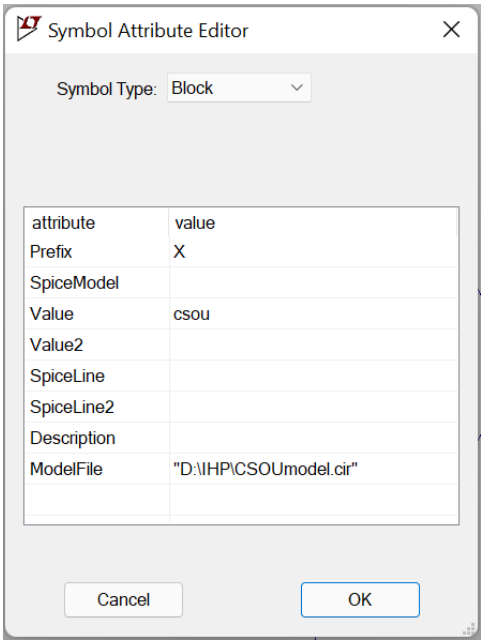


Fig. 11. Symbol attribute settings

15. Save the symbol with the assigned netlist in the same folder where the LTSpice project is located: File / Save As. The name of symbol can be „SET“. The file should have the extension * .asy.
16. In order to include the SET model in the simulation, you need to click on Components from the palette, and then select the path of the active project for the Top Directory, where we saved the SET model (Fig. 12). Choose a symbol and place it on the schematic (Fig. 13).

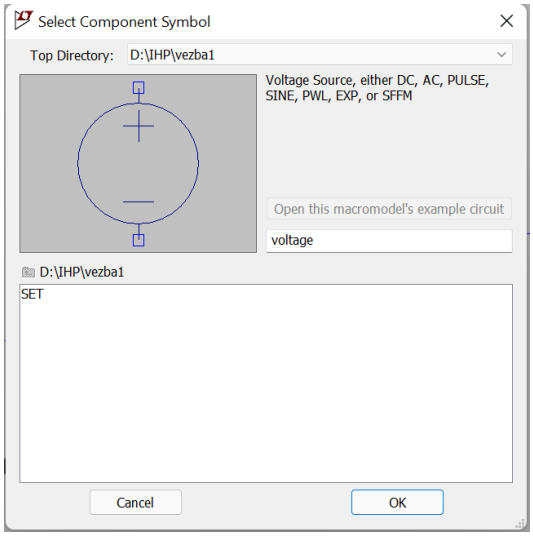


Fig. 12. Selection of component symbol

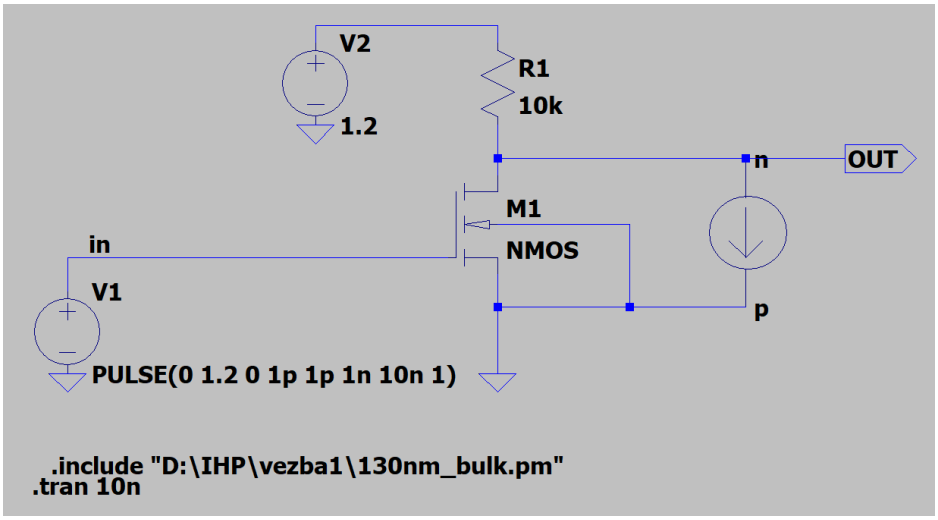


Fig. 13. Schematic with SET generator

17. It should be noted that the LET parameter in the SET model card is set as {let1}, which means that it is not assigned a default value. In the simulation, it is necessary to set the desired value of this parameter using the ***.params*** command, as shown in Fig. 14. To keep the transistor off, set generator V1 to 0V.

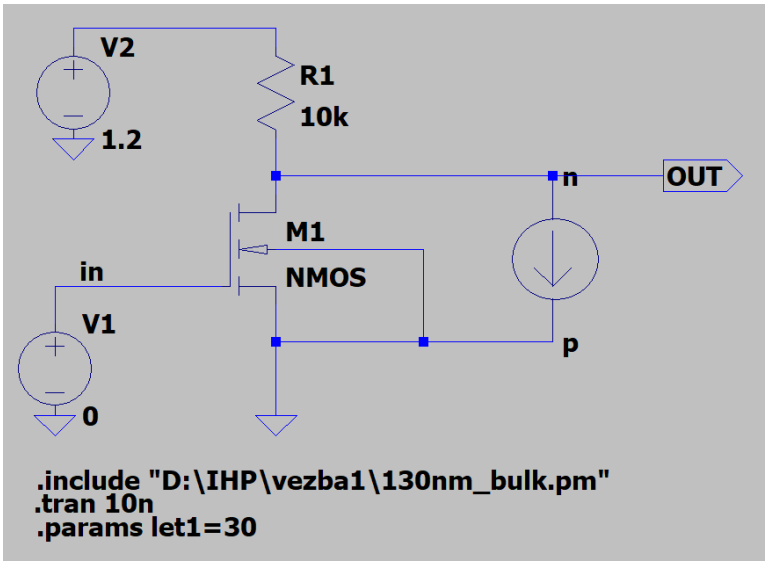


Fig. 14. Adding of ***.params*** directive

18. The simulation results for LET = 30 MeVcm$^2$mg$^{-1}$ are shown in Fig. 15. The SET current pulse (Ix (U1: n)) as well as the output voltage (V (out)) are shown. When the transistor is in the *off* state the output is a logic 1. Due to the appearance of SET, the transistor switches *on* for a short time and the signal at the output goes to the logic 0.

19. In order to analyze the behavior of the circuit for different LET values, we will perform a parametric analysis. The SPICE command ***.STEP PARAM*** is used for this purpose, as shown in Fig. 16. In this case, the LET value will change from 1 to 100 with step 10.
20. Run the simulation and observe the output signal (*out*). To display the legend: right click in the simulation results window, View / Step Legend. From Fig. 17 it can be concluded that with the increase of the LET value, the width of the generated pulse increases, ie. the transistor stays in *on* state longer because the SET-causing particles have more energy.

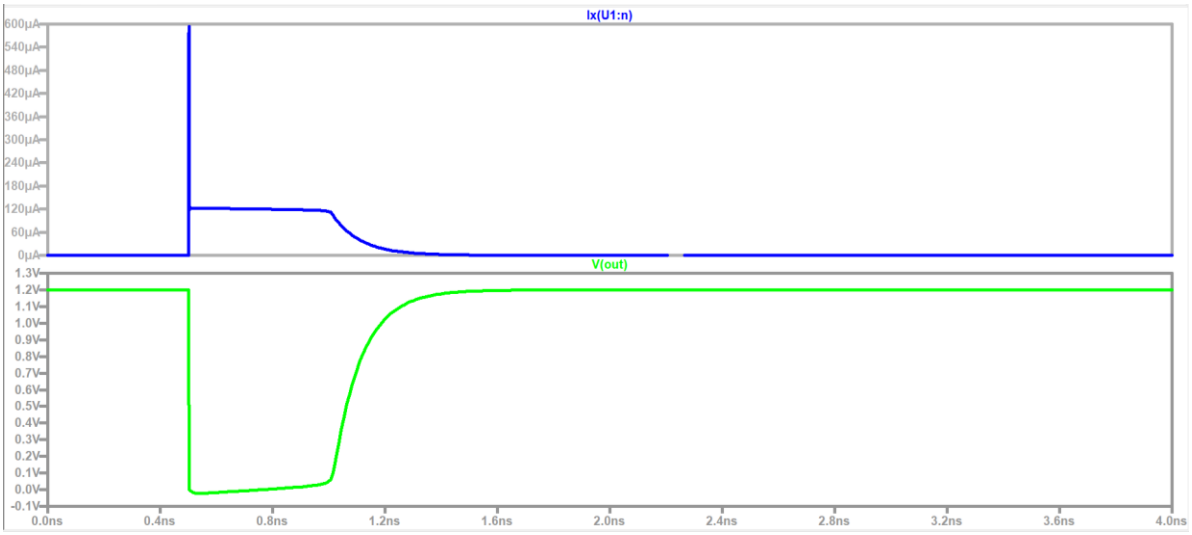


Fig. 15. Simulation results for LET=30 MeVcm$^2$mg$^{-1}$

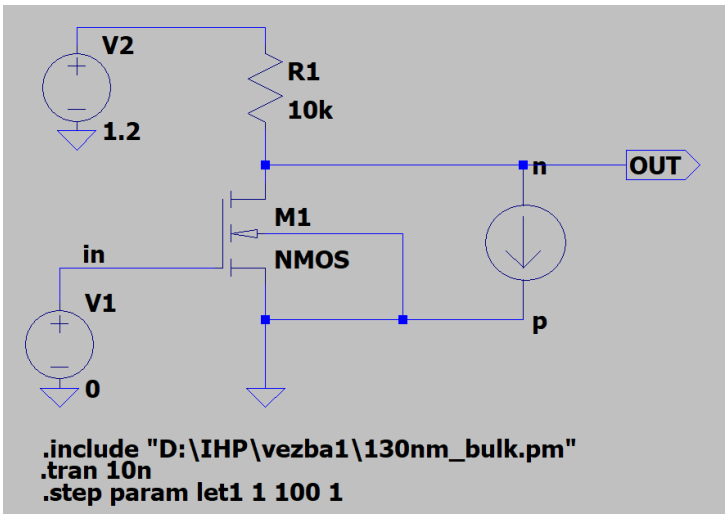


Fig. 16. Adding of ***.step param*** directive

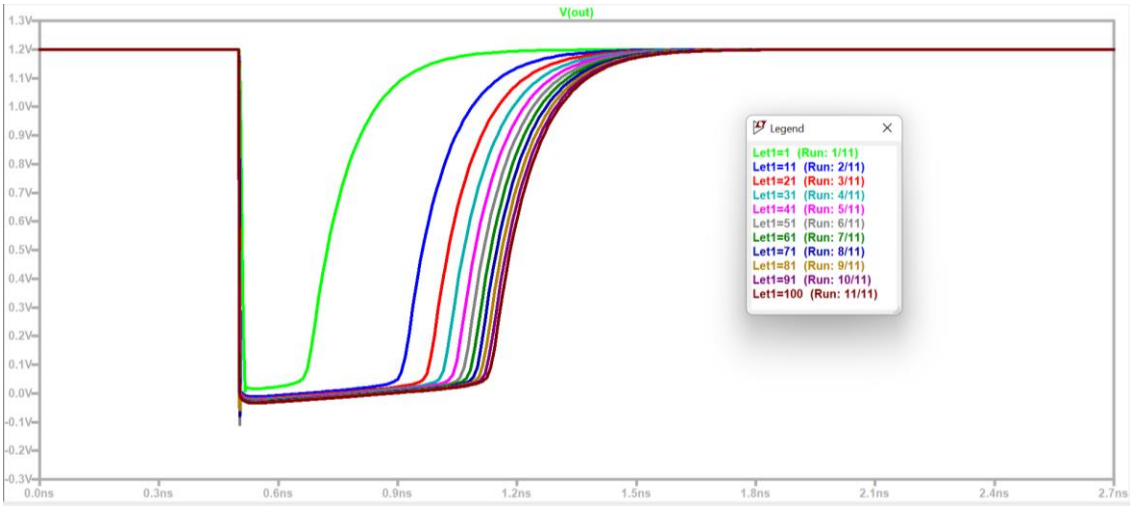


Fig. 17. Simulation results for different LET values

**Homework**

Repeat the described procedure of modeling and simulation of the SET effect on the example of PMOS transistors as switching components. Discuss simulation results without and with SET. Repeat the simulations for 1.1 and 1 V. Discuss the impact of supply voltage on SET pulse width.

**References**

[1] M. Andjelkovic, A. Ilic, Z. Stamenkovic, M. Krstic, and R. Kraemer, An overview of the Modeling and Simulation of the Single Event Transients at the Circuit Level, Proc. 30th International conference on microelectronics (MIEL 2017), Niš, Serbia, October, 9th-11th, 2017.

[2] J. S. Kauppila et al. A Bias-Dependent Single-Event Compact Model Implemented Into BSIM4 and a 90 nm CMOS Process Design Kit, IEEE Transactions on Nuclear Science, vol. 56, no. 6, December 2009.